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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,808	06/27/2003	Hae Jin Yun	041501-5583	5874

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EXAMINER	
AKKAPEDDI, PRASAD R	
ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 10/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,808	YUN, HAE JIN	
	Examiner	Art Unit	
	Prasad R Akkapeddi	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-27 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 27 June 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 10,11,15, 19 and 21 are objected to because of the following informalities: The following terms have no antecedent basis: 'C-shaped groove' in claim 10; 'the channel region' in claim 11; 'the metal layer' in claim 15; 'the second semiconductor layer, the channel region, the active layer' in claim 19; 'C-shaped groove' in claim 21. Appropriate correction is required.

2. Claim 23 is objected to because of the following informalities: The claim language recites "the passivation layer is formed of at least one inorganic insulating layer including silicon nitride or silicon oxide **and** an organic insulating layer including BenzocycloButene (BCB) or acrylic resin. Whereas, in the specification it is recited that the passivation layer is formed of at least one inorganic insulating layer including silicon nitride or silicon oxide **or** an organic insulating layer including BenzocycloButene (BCB) or acrylic resin (page 8, lines 15-17). It is not certain whether the passivation layer consists of at least one inorganic layer **and/or** an organic layer. Appropriate clarification is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-22 and 24-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim (U.S.Patent No. 5,790,222).

a. As to claim 1: Kim discloses a TFT-LCD with an insulating substrate (40), a gate line (42), a first data line (43) perpendicular to the gate line (42) and separated from the gate line by two or more insulating layers (col. 3, lines 8-9), a second data line (49) (upper data line) crossing the gate line (42) on a same line as the first data line (Fig. 4), a thin film transistor (TFT) at the crossing point of the gate line (42) and the second data line (49), an active layer (45, Fig. 5) below the second data line (49), a source electrode (47) and a drain electrode (48), a third data line (49) (lower data line) (col. 2, lines 19-20), disposed perpendicular to the gate line (42) and electrically connects the first and the second data lines with each other (thru contact holes T1 and T2 that can be seen in Fig. 4) and a pixel electrode (51) in the pixel region.

b. As to claims 2 and 3: In Fig. 5, Kim discloses that the gate electrode (41) which is an extension of gate line (42) and the data line (43) are on the same layer on top of the substrate and Kim in disclosing the prior art (col. 1, lines 14-15) teaches that the gate electrode is made from chromium.

c. As to claim 4: Kim shows in Fig. 5 that the first data line (43) is adjacent to the pixel electrode (51).

d. As to claim 5: Kim also discloses a passivation layer (50) formed over the entire surface of the insulating layer (44) including the second data line (49) (see Fig. 5).

e. As to claims 6 and 7: Kim discloses first, second and third contact holes (Fig. 4) on both sides of the first data line (43) and on both sides of the second data line (49) and at the drain electrode (48) and the connection of the data lines through the contact holes is disclosed in (col. 4, lines 33-53).

f. As to claim 8: Kim discloses that the thin film transistor (TFT) includes a source electrode (47) protruding from the second data line (49), a drain electrode (48) apart from the source electrode (47) and a gate electrode (41) extending from the gate line (42).

g. As to claims 9 and 10: The partial overlapping of the source electrode (47) and the drain electrode (48) on either side of the gate electrode (41) to define 'C'-shaped groove can be seen from Fig. 4.

h. As to claim 11: The ohmic contact layer (46) on the active layer (45) corresponding to the second data line (49), the source electrode (47) and the drain electrode (48) except the channel region is shown in Fig. 5

i. As to claims 12 and 13: Kim discloses a pixel electrode (51) made from ITO (col. 4, lines 50-51) and the location of the pixel electrode with the third data line (49) (lower) is disclosed in (col. 3, lines 40--59).

j. As to claim 14: The formation of the second data line (49) along with the source electrode (47) and drain electrode (49) via the deposition of an

amorphous silicon layer (45) and an n+ amorphous silicon layer (46) and a metal layer is disclosed in (col. 3, lines 24-36) and is shown in Fig. 5.

k. As to claim 15: Kim discloses a method of manufacturing the LCD device (col. 4, lines 8-67 and col. 5, lines 1-42) wherein the method includes a gate line (42), a first data line (43) perpendicular to the gate line (42) and separated from the gate line by two or more insulating layers (col. 3, lines 8-9), a second data line (49) (upper data line) crossing the gate line (42) on a same line as the first data line (Fig. 4), a thin film transistor (TFT) at the crossing point of the gate line (42) and the second data line (49), an active layer (45, Fig. 5) below the second data line (49), a source electrode (47) and a drain electrode (48), a third data line (49) (lower data line) (col. 2, lines 19-20), disposed perpendicular to the gate line (42) and electrically connects the first and the second data lines with each other (thru contact holes T1 and T2 that can be seen in Fig. 4) and a pixel electrode (51) in the pixel region.

l. As to claims 16 and 17: In Fig. 5, Kim discloses that the gate electrode (41) which is an extension of gate line (42) and the data line (43) are on the same layer on top of the substrate and Kim in disclosing the prior art (col. 1, lines 14-15) teaches that the gate electrode is made from chromium.

m. As to claim 18: Kim shows in Fig. 5 that the first data line (43) is adjacent to the pixel electrode (51).

n. As to claim 19: Kim discloses the patterning process by photolithography so that the thin film transistor (TFT) includes a source electrode (47) protruding

from the second data line (49), a drain electrode (48) apart from the source electrode (47) and a gate electrode (41) extending from the gate line (42). The formation of the second data line (49) along with the source electrode (47) and drain electrode (49) via the deposition of an amorphous silicon layer (45) and an n+ amorphous silicon layer (46) and a metal layer is disclosed in (col. 3, lines 24-36) and is shown in Fig. 5. (col.4, lines 8-46).

o. As to claims 20 and 21: The partial overlapping of the source electrode (47) and the drain electrode (48) on either side of the gate electrode (41) to define 'C'-shaped groove can be seen from Fig. 4.

p. As to claim 22: Kim also discloses a passivation layer (50) formed over the entire surface of the insulating layer (44) including the second data line (49) (see Fig. 5).

q. As to claims 24 and 25: Kim discloses first, second and third contact holes (Fig. 4) on both sides of the first data line (43) and on both sides of the second data line (49) and at the drain electrode (48) and the connection of the data lines through the contact holes is disclosed in (col. 4, lines 33-53).

r. As to claims 26 and 27: Kim discloses a pixel electrode (51) made from ITO (col. 4, lines 50-51) and the location of the pixel electrode with the third data line (49) (lower) is disclosed in (col. 3, lines 40--59).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Kim et al. (Kim 2) (U.S.Patent No. 6,100,953).

As to claim 23: Although passivation layers consisting of inorganic and/or organic layers are quite commonly used in liquid crystal displays, and Kim also teaches the use of passivation film (50) on the second data line (49), Kim does not disclose that the passivation film consists of at least one inorganic insulating layer including silicon nitride or silicon oxide and an organic insulating layer including BenzocycloButene (BCB) or acrylic resin.

Kim 2, in disclosing a liquid crystal device teaches that the passivation layer includes BCB, acrylic resin, polyimide compound in addition to silicon nitride or silicon oxide (col. 6, lines 33-34 and 44-46).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to adapt the silicon nitride, silicon oxide or the BCB as the material of choice for passivation layer in order to prevent various electrodes from interfering with the distorting electric fields from other electrodes (col. 6,lines 27-31).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prasad R Akkapeddi whose telephone number is 571-272-2285. The examiner can normally be reached on 7:00AM to 5:30PM M-Th.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H Kim can be reached on 571-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Prasad R Akkapeddi, Ph.D
Examiner
Art Unit 2871

PRA

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TARIFUR R. CHOWDHURY
PRIMARY EXAMINER